Tobias Nardmann

Physics-based compact modeling and parameter extraction for InP heterojunction bipolar transistors with special emphasis on material-specific physical effects and geometry scaling

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Physics-based compact modeling and parameter extraction for InP heterojunction bipolar transistors with special emphasis on material-specific physical effects and geometry scaling

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**Für meine Eltern
und für Julia.**

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Abstract

Given the increasing interest in both high-frequency and high-power applications, III-V HBTs and especially devices based on InP - which can be faster than SiGe HBTs and retain a better power-handling capability - have the potential to fill an important demand in the microelectronics world. Already, such transistors have achieved maximum oscillation frequencies beyond 1 THz. A major obstacle for more widespread deployment of III-V technologies is the lack of systematic process scaling, compact modeling and model parameter extraction. III-V foundries generally offer a limited number of device sizes with individual (i.e. non-scalable) model cards for each of them. Thus, circuit designers cannot freely choose device sizes. Additionally, physics-based modeling is not a high priority, with self-heating - the main breakdown mechanism for III-V HBTs - commonly being disregarded. Finally, the formulations for dedicated III-V compact models are based on those found in the SGPM model and cannot include all necessary physical effects in a consistent way. These factors combine to prevent circuits designed in III-V technologies from reaching their full potential.

Based on an analysis of the device structure and material properties, the most important differences between III-V and SiGe HBTs are identified with the goal of developing extensions for modern compact models used for SiGe and enabling them to model also III-V devices. The HICUM compact model is chosen as a basis for this work. The impact of the NDM effect on the collector charge and the doping- and composition grading on the junction capacitance require an extension of the compact model code, which is performed in a physics-based way consistent with existing model formulation.

The parameter extraction is investigated, with a special focus on the series resistance extraction, which often employs so-called extraction methods for determining the resistance value based on terminal data from a single transistor. Those methods are evaluated using compact-model generated data with a known target value. This evaluation is based on three separate InP HBT processes for which compact models were generated. Suitable methods are identified and some improvements are suggested. An extraction example for all relevant model parameters for single-transistor extraction is shown.

An approach for scalable parameter extraction, typical for SiGe devices, but uncommon for III-V HBTs, is applied to a 250 GHz InP HBT technology. Test structures for many technology parameters have been fabricated and are evaluated in order to increase the physical accuracy of the model parameters. Problems with the scaling approach are discussed based on deviation between the assumed and the actual device dimensions, indicating a need for a more stable fabrication process.

Finally, a comparison between the compact model and measured data is shown for the scalable model based on the 250 GHz InP technology, for the fastest commercially available InP technology with $f_{\max} > 500$ GHz and for a 80 GHz GaAs technology.

Kurzfassung

Durch das stetig steigende Interesse an Schaltungen, die sowohl bei hohen Frequenzen als auch bei hohen Leistungen arbeiten, haben III-V HBTs - insbesondere mit dem Basismaterial InP, die schneller als SiGe HBTs arbeiten und dennoch eine höhere Durchbruchspannung aufweisen - das Potential, eine wichtige Lücke in der Mikroelektronik zu füllen. Solche Transistoren haben bereits Oszillationsfrequenzen oberhalb von 1 THz erreicht. Ein wichtiges Hindernis für die großflächige Anwendung von III-V-Technologien ist der Mangel an einem systematisch verwendeten Ansatz für die Skalierung von Prozessen, die Modellierung der Bauelemente und die Extraktion von Parametern für die Modelle. III-V-Hersteller bieten generell eine eingeschränkte Zahl von Transistoren an, für die individuelle - also nicht skalierbare - Modellparametersätze erstellt wurden. Schaltungsentwickler können also die Maße der zu verwendenden Transistoren nicht frei wählen. Darüber hinaus ist die physikbasierte Modellierung der Bauelemente meist keine Priorität für die Hersteller; sogar die Selbsterhitzung der Transistoren, die oft die Ursache für die Zerstörung der Bauelemente ist, wird häufig nicht mit einbezogen. Weiterhin basieren die Gleichungen der Kompaktmodelle, die spezifisch für III-V HBTs entwickelt wurden, auf dem SGPM-Modell und enthalten nicht alle relevanten physikalischen Effekte. Die Kombination dieser Faktoren verhindert, dass das Potential von III-V-Technologien voll ausgeschöpft werden kann.

Basierend auf einer Analyse der Materialien und Strukturen werden die wichtigsten Unterschiede zwischen III-V und SiGe-HBTs identifiziert. Das Ziel der Analyse ist, Erweiterungen für moderne SiGe HBT Kompaktmodelle zu entwickeln und diese damit in die Lage zu versetzen, auch III-V HBTs modellieren zu können. Das Kompaktmodell HICUM wird als Grundlage für diese Arbeit verwendet. Durch den Einfluß des NDM-Effekts auf die Kollektorladung und des Dotierungs- bzw. Materialübergangs auf die Sperrschichtkapazität werden neue Gleichungssysteme für das Modell benötigt. Die entwickelten Gleichungen sind physikbasiert und die Formulierung ist konsistent mit dem aktuellen Modell.

Die Extraktion der Modellparameter wird mit einem besonderen Fokus auf die Serienwiderstände untersucht. Letztere werden oft unter Verwendung von sog. Extraktionsmethoden durchgeführt, die messbare Klemmendaten eines einzelnen Tranistors direkt mit einem Widerstand in Verbindung brin-

gen. Diese Methoden werden auf der Basis von modellgenerierten Daten mit einem bekannten Sollwert ausgewertet, was eine Bewertung der Genauigkeit ermöglicht. Einige Verbesserungen für Methoden werden vorgeschlagen. Beispiele für die Extraktion aller relevanten Modellparameter werden auf der Basis von Einzeltransistor-Extraktion gezeigt.

Ein Ansatz für die skalierbare Parameterextraktion wie er typischerweise für SiGe HBTs, aber selten für III-V HBTs durchgeführt wird, wird für eine 250 GHz InP HBT Technologie implementiert. Teststrukturen für zahlreiche Technologieparameter wurden hergestellt und werden ausgewertet, um den physikalischen Bezug des Modellparametersatzes zu verbessern. Probleme mit dem Skalierungsansatz werden auf Basis der Differenz der erwarteten und tatsächlichen Transistordimensionen diskutiert; diese Differenz impliziert, dass stabielere Produktionsprozesse benötigt werden.

Abschließend wird ein Vergleich zwischen Modellergebnissen und Messdaten für die 250 GHz InP Technologie, die schnellsten kommerziell verfügbaren InP Transistoren mit $f_{\mathrm{max}} > 500\,\mathrm{GHz}$ und eine 80 GHz GaAs Technologie gezeigt.

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List of Symbols

Abbreviations

(C)MOS	(Complementary) metal oxide semiconductor
B, C, E, S	Base, collector, emitter, substrate
BE, BC, CE	Base-emitter, Base-collector, collector-emitter
BJT	Bipolar Junction Transistor
CMC	Compact Model Coalition
CNTFET	Carbon nanotube field effect transistor
DD	Drift-diffusion
EC	Equivalent circuit
FOM	Figure of merit
GaAs	Gallium arsenide
GICCR	Generalized integral charge control relation
HBT	Heterojunction Bipolar Transistors
HD	Hydrodynamic
HEMT	High electron mobility transistor
HICUM	The HICUM bipolar transistor model. High current model
HV	High voltage
IC	Integrated circuit
III-V	Material consisting of elements from the third and fifth main group of elements
InGaAs	Indium gallium arsenide
InP	Indium phosphide
MOSFET	Metal-oxide-semiconductor field effect transistor

RF	Radio frequency
SCR	Space charge region
SEM	Scanning electron microscopy
SGP	Spice Gummel Poon
Si, Ge, SiGe	Silicon, germanium, silicon germanium
SIMS	Secondary ion mass spectroscopy
TEM	Transmission electron microscopy
VA	Verilog-A

Constants

$\mathrm{m_0}$	Electron mass
ε_0	Vacuum permittivity
$\mathrm{k_B}$	Boltzmann constant
q	Elementary charge

Variables

β_f	Forward small-signal current gain
B_f	Forward DC current gain
C_BE, C_BC, C_CE	Terminal base-emitter, base-collector and collector-emitter capacitance
C_dEi, C_dCi	Internal base-emitter and base-collector diffusion capacitance
C_jEi, C_jCi	Internal base-emitter and base-collector junction capacitance
$E_\mathrm{jC}, E_\mathrm{wC}$	Electric field at the BC junction and at collector-subcollector transition
f_t, f_max	Cutoff frequency and maximum oscillation frequency
I_BE, I_BC	Currents flowing through the base-emitte resp. base-collector diode
I_B, I_C, I_E	Terminal base, collector and emitter current
I_T, J_T	Transfer current, transfer current density
J_B, J_C, J_E	Terminal base, collector and emitter current density
N_B, N_C, N_E	Doping concentration in base, collector and emitter
Q_jEi, Q_jCi	Internal base-emitter and base-collector junction charge

Q_{p0}, Q_{p}	(Zero-bias) hole charge
R_{Bi}, R_{Bx}, R_{B}	Internal, external and total base resistance
R_{Cx}, R_{E}	Collector and emitter series resistance
R_{th}	Thermal resistance
T_0, T	(Reference) temperature
$V_{\mathrm{B'E'}}$, $V_{\mathrm{B'C'}}$, $V_{\mathrm{C'E'}}$	Internal base-emitter, base-collector and collector-emitter voltages
V_{BE}, V_{BC}, V_{CE}	Terminal base-emitter, base-collector and collector-emitter voltages
V_{Ci}	Internal collector voltage
V_{T}	Thermal voltage
w_{BC}	Collector SCR width
w_{c}	Collector width

CHAPTER 1

Introduction

The trend in modern electronics towards ever higher frequencies of operation and complexity as well as power efficiency requires a broad palette of different technologies to be available to circuit designers for various applications. While metal-oxide-semiconductor field effect transistors (MOSFETs) dominate the digital world, they have apparently reached their top analog performance around the 65 nm node [SUZC15, VTD+13]. Emerging technologies such as carbon nanotube field effect transistors (CNTFETs) theoretically offer excellent properties such as very high linearity and speed, but have yet to deliver on those promises in practice [SCS+13]; the measured transit frequency (f_T) of emerging devices rarely exceeds approximately 10 GHz [SKW+11] due to the impact of series resistances, parasitical capacitances and other unwanted effects.

Heterojunction bipolar transistors (HBTs), on the other hand, offer a number of key advantages over competing technologies: a very high transconductance and therefore a relatively low impact of a load impedance on the transistor operation [SUZC15], a high transit frequency (f_T) and maximum frequency of oscillation (f_max) at a comparatively relaxed lithography and favorable noise characteristics.

Like all semiconductor devices, HBTs can be fabricated in different semiconductor materials. The most common are silicon-germanium (SiGe) HBTs, which even today reach values above $(f_\mathrm{T}, f_\mathrm{max}) = (505,\ 720)$ GHz ([HRB+16]) and are projected to eventually reach the THz range ([SWH+11]). SiGe HBTs are easily integrable with MOSFETs in so-called BiCMOS processes, which utilize the advantages of both technologies.

However, HBTs fabricated in III-V materials (i.e. semiconductors consisting of one element of the third and one of the fifth main group of elements) offer a versatile alternative. Depending on the materials that are used, III-V HBTs can be the fastest available bipolar transistors [UPR+11] (competing only with high electron mobility transistors (HEMTs), also fabricated in III-V materials, for the title of fastest available transistors overall), offer very high breakdown voltages and therefore excellent power-handling capability and show good linearity [WMX+06] and low noise figures at high frequencies [SS13]. The importance of a possible integration with a complementary MOS (CMOS) process in Silicon has also been recognized in the III-V community and been the subject of some research in recent years [Kaz13]. Typical applications for III-V HBTs include handset power amplifiers (PAs) (e.g. [MdRZ13]), high-efficiency [GURP15] and high-speed [RRG+12] amplifiers as well as high-speed oscillators [SUH+11]. Overall, III-V-based HBTs and especially Indium-Phosphide (InP) HBTs are excellent candidates for future high-speed communication circuits.

In order to fully utilize the capabilities of any transistor technology in circuit design, a good compact model is needed. A compact model allows the prediction of circuit performance ahead of fabrication, thus saving time and money by reducing design iterations. Similarly, a model that agrees very well with the actual device performance allows slimmer safety margins and therefore more optimized circuits. If the model is physics-based, that is, if its EC elements have a direct physical relation to a region of the device and its parameters can be determined from material properties, physical constants and the device geometry, it can also be used for predictive modeling, i.e. predicting the performance of future devices with some confidence. Its parameters can be determined in a relatively low frequency range, typically several GHz, while retaining accuracy up to frequency ranges where experimental characterization is difficult for small-signal and impossible for large-signal operation. Furthermore, a scalable compact model that is able to determine the device performance for nearly arbitrary sizes and configurations of transistors helps designers choose exactly the device that is needed, thus reducing power dissipation, and can even be used in circuit optimization routines.

Unfortunately, compact modeling of III-V HBTs is not on a level comparable with what is common in the silicon world. The lack of accurate transistor models is a major obstacle for deploying InP technology in production circuit design (e.g. [HZC+07], [Zir12]) and is documented by various attempts to improve existing compact models (e.g. [IRS+03], [NMPG09]). The most widely used compact model for III-V HBTs, the Agilent HBT model (AHBT) [Agi16], is based on the UCSD HBT model [UCS00], which is itself built on the Spice Gummel-Poon (SGPM) model [GP70] and does not contain physics-

based formulations for multiple effects typically encountered in modern HBTs. Additionally, despite notable exceptions [HZC+07], the use of test structures for the accurate determination of compact model parameters is uncommon. However, models intended for the SiGe material system cannot necessarily be used for III-V HBTs directly due to unique physical effects occuring in the materials as well as the vertical and lateral structure employed in their manufacture.

The goal of this work is to include important effects occurring in III-V materials in a compact model for circuit design in a physical, yet intuitive way in order to aid deployment of III-V HBTs in prototypes and products. The HICUM compact model [SC10] was chosen as a basis, since, along with MEXTRAM, it is one of two models supported by the Compact Modeling Coalition (CMC) as an industry standard and has been widely deployed in process design kits (PDKs) for years by semiconductor manufacturers around the world. The model is in constant development, striving to include new physical effects as they become important due to increasingly aggressive vertical and lateral scaling, but to date no comprehensive effort to include the effects typical for III-V materials was made. However, the models derived for physical effects in this work are applicable not only in HICUM, but for compact modeling in general. Similarly, the approaches for parameter determination for, e.g., the series resistances, the area-perimeter separation or the junction diodes are not model-specific.

This thesis is structured as follows: In chapter 2, basic principles of compact modeling and the expected differences between HBTs manufactured in the SiGe respectively III-V material systems are discussed. A summary of the changes made to the standard HICUM/L2 model is given in chapter 3. Chapter 4 focuses on the determination of model parameters from both test structures and single transistor extraction methods, providing examples for the various steps as a guide to modeling III-V HBTs, before a comparison between model and measured data for multiple technologies is shown in chapter 5. Finally, a summary of this work as well as an outlook on future work is given in chapter 6.

CHAPTER 2

Modeling III-V based HBTs

2.1 Introduction

In this chapter, general principles of compact modeling as well as compact modeling specifically with a focus on III-V HBTs are discussed. Numerical device simulation as an important tool for understanding device physics is also briefly addressed.

In order to use some of the advantages of compact modeling, a physical basis for the models is required. This allows linking a certain measured device behavior to the appropriate parameters, enabling, e.g., scaling of the model. While many physical principles in SiGe and III-V HBTs are very similar (e.g. injection of minority carriers from the emitter into the base and subsequent transport into the collector), there are a number of differences caused by both the material itself as well as the transistor cross-section typically in use. The most relevant differences are summarized in 2.2.

Compact models for electron devices form the link between the semiconductor technology and circuit design. In modern circuits, it is impossible to accurately predict the circuit performance without the aid of computer-aided design (CAD) tools. Iterating designs over multiple wafer runs to optimize performance is prohibitively expensive and time-consuming. Simultaneously, numerical device simulations are not only too time-intensive, but also too inflexible to be used in circuit design since they rely not on extractable parameters, but a known doping profile and material parameters and serve better as a tool for understanding the semiconductor physics in principle. Physics-based compact models, which can be used in a circuit simulator, form an ideal mid-

dle ground for circuit design. They can also have additional functionality in predictive and statistical modeling, allowing yield prediction and even process debugging. The basic principles of compact modeling are discussed in section 2.3.

While device measurements are the ultimate reference for a compact model, numerical semiconductor device simulations are a very useful tool. They allow an investigation of the status within the device by solving the differential equations (depending on desired complexity and physical accuracy the drift-diffusion (DD), hydrodynamic (HD) or Boltzmann transport equation (BTE) systems for HBT simulations) describing the device behavior based on technological data such as doping profiles, known material data and biasing. If all input parameters are accurately known and all relevant physical effects are included, the solution is very accurate. For compact modeling, these device simulations are a powerful tool for understanding the devices and verifying model simplifications. Section 2.4 briefly discusses the application of numerical simulations to III-V materials.

2.2 Differences between SiGe and III-V HBTs

This section discusses the differences between SiGe and III-V HBTs. These differences indicate which additional effects may have to be taken into account in the compact model. This work assumes that the reader is familiar with the basic operation of a bipolar junction transistor (BJT) and heterojunction bipolar transistor (HBT) and does not discuss their physical background in depth. The interested reader is referred to the literature, such as [SC10, Rud06]. Instead, only major differences in III-V materials and cross-sections and their expected impact on a compact model are described.

Three categories will be investigated: The properties of III-V materials, the vertical doping and material profile and the lateral geometry. The latter primarily affects scaling equations and has an impact on the relative quantities of certain equivalent circuit elements; the former two can have a direct impact on the physical description of the device.

2.2.1 III-V material properties

2.2.1.1 Electron and hole mobilities

HBTs can be fabricated as npn-devices, where electrons as minorities in the base carry the transfer current, and as pnp-devices, in which holes are mainly responsible for the current transport. Complementary devices are especially useful in many types of digital circuits. While both types of devices can also